Listing of Claims:

1. (Previously Presented) A programmable buffer circuit for interfacing a CPU to a plurality of channel interfaces, comprising:

a single dual port memory having a first port coupled to a CPU data bus and a second port coupled to a channel data bus that serves said plurality of channel interfaces;

an arbitrator for arbitrating access to said dual port memory by individual ones of said channel interfaces over said channel data bus for selectively storing data in and reading data from said single dual port memory;

an address generator for generating dual port memory addresses for selectively reading data from and writing data to said single dual port memory using said CPU data bus and said channel data bus; and

an allocator and control unit programmable by said CPU for specifying individual ones of buffer locations and buffer sizes within said single dual port memory for individual ones of said channel interfaces, and for enabling individual ones of said buffers, said allocator having outputs coupled to said address generator for controlling the generation of addresses thereby depending on which channel interface is currently selected for access to said single dual port memory, wherein in a first case said control unit operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and in a second case said control unit operates said individual ones of channel buffers in a first in/first out (FIFO) access mode of operation using said same set of channel registers.

2. (Canceled)

3. (Original) A programmable buffer circuit as in claim 1, wherein at least said dual port memory,

said CPU and said plurality of interface channels are contained within a common integrated circuit package.

4. (Original) A programmable buffer circuit as in claim 1, wherein one of said plurality of interface channels is comprised of an audio CODEC.

5. (Original) A programmable buffer circuit as in claim 1, wherein one of said plurality of interface channels is comprised of a serial data interface.

6. (Original) A programmable buffer circuit as in claim 1, wherein one of said plurality of interface channels is comprised of a packet data interface channel.

7. (Previously Presented) A programmable buffer circuit as in claim 1, wherein individual ones of said plurality of interface channels are comprised of a receive interface and a transmit interface, and wherein said allocator comprises a corresponding plurality of registers for specifying at least a starting address and a size for each of said receive interface and said transmit interface.

8. (Original) A programmable buffer circuit as in claim 1, wherein individual ones of said plurality of interface channels are comprised of a receive interface and a transmit interface, and wherein said buffer circuit is programmable for specifying a receive buffer of one channel interface to be a transmit buffer of another channel interface.

9. (Previously Presented) A method for operating a programmable buffer circuit for interfacing a CPU to a plurality of channel interfaces, comprising:

providing a single dual port memory having a first port coupled to a CPU data bus and a second port coupled to a channel data bus that serves said plurality of channel interfaces;

programming a control unit for specifying a set of channel registers individual ones of

buffer locations and buffer sizes within said single dual port memory for individual ones of said channel interfaces and using said set of channel registers in a first case to operate individual ones of channel buffers in a block access mode and in a second case using said same set of channel registers to operate said individual ones of channel buffers in a first in/first out (FIFO) access mode of operation;

arbitrating for access to said single dual port memory by individual ones of said channel interfaces over said channel data bus; and

generating dual port memory addresses for selectively reading data from and writing data to said single dual port memory using said CPU data bus and said channel data bus, the generation of said addresses depending on which channel interface is currently selected for access to said dual port memory, and on the specified buffer location and size within said dual port memory for the selected one of said channel interfaces.

10. (canceled)

11. (Original) A method as in claim 9, wherein at least said dual port memory, said CPU and said plurality of interface channels are contained within a common integrated circuit package.

12. (Original) A method as in claim 9, wherein one of said plurality of interface channels is comprised of an audio CODEC, and wherein another one of said plurality of interface channels is comprised of at least one of a serial data interface and a packet data interface.

13. (Previously presented) A method as in claim 9, wherein individual ones of said plurality of interface channels are comprised of a receive interface and a transmit interface, and wherein programming specifies at least a starting address and a size for each of said receive interface and said transmit interface.

14. (Original) A method as in claim 9, wherein individual ones of said plurality of interface channels are comprised of a receive interface and a transmit interface, and wherein said step of programming specifies a receive buffer of one channel interface to be a transmit buffer of another channel interface.

15. (Previously Presented) A programmable buffer circuit for interfacing a data processor to a plurality of channel interfaces, comprising:

a single dual port memory having a first port coupled to a processor data bus and a second port coupled to a channel data bus that serves said plurality of channel interfaces;

an arbitrator for arbitrating access to said dual port memory by individual ones of said channel interfaces over said channel data bus for at least one of reading data from and for writing data to said dual port memory;

an address generator for generating dual port memory addresses for at least one of reading data from and writing data to said dual port memory using said data processor data bus and said channel data bus; and

a control unit programmable by said data processor for specifying for individual ones of buffers both buffer locations and buffer sizes within said single dual port memory for individual ones of said channel interfaces, where said control unit is programmable in a first case for operating individual ones of said buffers in a block access mode of operation and operating in a second case said individual ones of said buffers in a first in/first out (FIFO) access mode of operation using said same set of channel registers.

16. (Previously Presented) A programmable buffer circuit as in claim 15, wherein individual ones of said plurality of interface channels are comprised of a receive interface and a transmit interface, and wherein said buffer circuit is programmable for specifying a receive buffer of one

channel interface to be a transmit buffer of another channel interface.

17. (Previously Presented) A programmable buffer circuit for interfacing a data processor to a plurality of channel interfaces, comprising:

a dual port memory having a first port coupled to a processor data bus and a second port coupled to a channel data bus that serves said plurality of channel interfaces;

an arbitrator for arbitrating access to said dual port memory by individual ones of said channel interfaces over said channel data bus for at least one of reading data from and for writing data to said dual port memory;

an address generator for generating dual port memory addresses for at least one of reading data from and writing data to said dual port memory using said data processor data bus and said channel data bus; and

a control unit programmable by said data processor for specifying individual ones of buffer locations and buffer sizes within said dual port memory for individual ones of said channel interfaces, where there are four transmit registers allocated for each channel interface designated as BaseReg0, BaseReg1, SizeReg0 and SizeReg1 and four receive registers also designated as BaseReg0, BaseReg1, SizeReg0 and SizeReg1, said control unit being responsive to operating in a Block Mode to provide two independent buffers Buffer0 and Buffer1, where BaseReg0 stores the starting address of Buffer0, SizeReg0 specifies the size of Buffer0, BaseReg1 stores the starting address of Buffer1, and SizeReg1 specifies the size of Buffer1 size, said control unit being further responsive to operating in a FIFO Mode to provide one buffer, where BaseReg0 stores the start address of the single buffer, SizeReg0 specifies the size of the single buffer, BaseReg1 functions as a Low Threshold Register, and said register SizeReg1 functions as a High Threshold Register.

18. (Canceled)

19. (Previously Presented) A programmable buffer circuit for interfacing a data processor to a plurality of channel interfaces, comprising:

a dual port memory having a first port coupled to a processor data bus and a second port coupled to a channel data bus that serves said plurality of channel interfaces;

an arbitrator for arbitrating access to said dual port memory by individual ones of said channel interfaces over said channel data bus for selectively reading data from and writing data to said dual port memory;

an address generator for generating dual port memory addresses for selectively reading data from and writing data to said dual port memory using said processor data bus and said channel data bus; and

a control unit programmable by said data processor for specifying individual ones of buffer locations and buffer sizes within said dual port memory for individual ones of said channel interfaces, where said control unit is operable to set up and operate a first portion of said dual port memory in a block mode of operation having a transmit buffer and a receive buffer, and to also operate a second portion of the dual port memory in a FIFO mode of operation having a single buffer wherein a single set of channel registers controls the operation in said block mode and in said FIFO mode.

20. (Previously Presented) A programmable buffer circuit as in claim 19, where said first portion of said dual port memory is coupled to a data packet channel interface, and where said second portion of said dual port memory is coupled to an audio CODEC.

21. (Previously presented) A programmable buffer circuit for interfacing a CPU to a plurality of channel interfaces, comprising:

a single dual port memory having a first port coupled to a CPU data bus and a second port coupled to a channel data bus that serves said plurality of channel interfaces;

means for arbitrating access to said dual port memory by individual ones of said channel interfaces over said channel data bus for selectively storing data in and reading data from said single dual port memory;

means for generating dual port memory addresses for selectively reading data from and writing data to said single dual port memory using said CPU data bus and said channel data bus; and

means for allocating and means for controlling programmable by said CPU for specifying individual ones of buffer locations and buffer sizes within said single dual port memory for individual ones of said channel interfaces, and for enabling individual ones of said buffers, said allocator means having outputs coupled to said address generating means for controlling the generation of addresses thereby depending on which channel interface is currently selected for access to said single dual port memory, wherein in a first case said controlling means operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and in a second case said controlling means unit operates said individual ones of channel buffers in a first in/first out (FIFO) access mode of operation using said same set of channel registers.

22. (Previously presented) The programmable buffer circuit of claim 17 wherein at least said dual port memory and said plurality of channel interfaces are contained within a common integrated circuit package.

23. (canceled)

24. (canceled)